深圳市集芯源电子科技有限公司

Cost-Effective A/D Flash 8-Bit MCU with EEPROM

JXY-FC08

Revision: V1.50 Date: November 27, 2015

Note that 8-pin MCU package types are not marketed in the following countries: USA, UK, Germany, The Netherlands, France and Italy.

Features

CPU Features

- Operating Voltage
  - f_{SYS} = 8MHz: 2.2V~5.5V
- Up to 0.5μs instruction cycle with 8MHz system clock at V_{DD}=5V
- Power down and wake-up functions to reduce power consumption
- Two Oscillators
  - Internal RC -- HIRC
  - Internal 32kHz -- LIRC
- Fully intergrated internal 8MHz oscillator requires no external components
- Multi-mode operation: NORMAL, SLOW, IDLE and SLEEP
- All instructions executed in one or two instruction cycles
- Table read instructions
- 63 powerful instructions
- Up to 4-level subroutine nesting
- Bit manipulation instruction

Peripheral Features

- Flash Program Memory: 1K×14/2K×15
- RAM Data Memory: 64×8/96×8
- EEPROM Memory: 32×8
- Watchdog Timer function
- Up to 18 bidirectional I/O lines
- Software controlled 4-SCOM lines LCD driver with 1/2 bias (only available for HT66F004)
- Multiple pin-shared external interrupts
- Multiple Timer Modules for time measure, compare match output, capture input, PWM output, single pulse output functions
- Dual Time-Base functions for generation of fixed time interrupt signals
- Multi-channel 12-bit resolution A/D converter
- Low voltage reset function
- Wide range of available package types
- Flash program memory can be re-programmed up to 100,000 times
- Flash program memory data retention > 10 years
- EEPROM data memory can be re-programmed up to 1,000,000 times
- EEPROM data memory data retention > 10 years

General Description

The devices are Flash Memory type 8-bit high performance RISC architecture microcontrollers. Offering users the convenience of Flash Memory multi-programming features, these devices also include a wide range of functions and features. Other memory includes an area of RAM Data Memory as well as an area of EEPROM memory for storage of non-volatile data such as serial numbers, calibration data etc.

Analog features include a multi-channel 12-bit A/D converter function. Multiple and extremely flexible Timer Modules provide timing, pulse generation, capture input, compare match output, single pulse output and PWM generation functions. Protective features such as an internal Watchdog Timer and Low Voltage Reset coupled with excellent noise immunity and ESD protection ensure that reliable operation is maintained in hostile electrical environments.

A full choice of HIRC and LIRC oscillator functions are provided including a fully integrated system oscillator which requires no external components for its implementation.

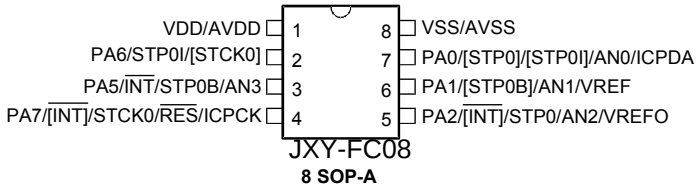
The inclusion of flexible I/O programming features, Time-Base functions along with many other features ensure that the devices will find excellent use in applications such as electronic metering, environmental monitoring, handheld instruments, household appliances, electronically controlled tools, motor driving in addition to many others.

Selection Table

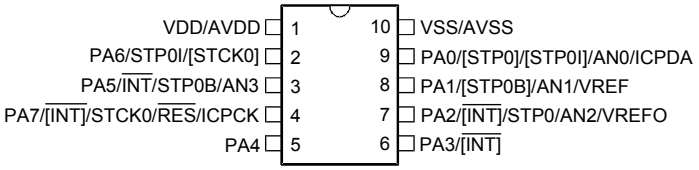
Most features are common to all devices, the main feature distinguishing them are Program Memory and Data memory capacity. The following table summarises the main features of each device.

Part No.	Program Memory	Data Memory	Data EEPROM	I/O	A/D Converter	Timer Module	Time Base	Stack	R-Type LCD	Package
JXY-FC08	1K×14	64×8	32×8	8	12-bit×4	10-bit STM×1	2	2	—	8SOP/ 10MSOP

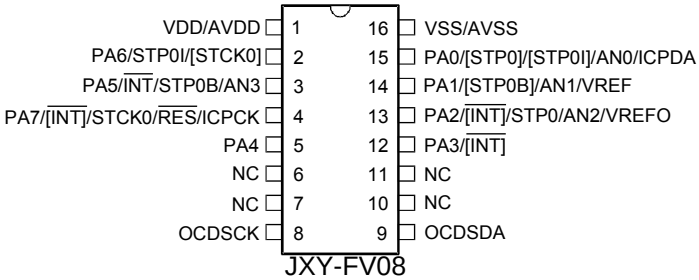
Pin Assignment



8 SOP-A



10 MSOP-A



16 NSOP-A

Pin Description

With the exception of the power pins and some relevant transformer control pins, all pins on these devices can be referenced by their Port name, e.g. PA0, PA1 etc, which refer to the digital I/O function of the pins. However these Port pins are also shared with other function such as the Analog to Digital Converter, Timer Module pins etc. The function of each pin is listed in the following table, however the details behind how each pin is configured is contained in other sections of the datasheet.

Pin Name	Function	OPT	I/T	O/T	Description
PA0/[STP0]/ [STP0I]/AN0/ ICPDA	PA0	PAWU PAPU PASR	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	STP0	PASR	—	CMOS	TM0 (STM) output
	STP0I	PASR IFS0	ST	—	TM0 (STM) input
	AN0	PASR	AN	—	ADC input channel 0
	ICPDA	—	ST	CMOS	ICP Data Line
PA1/[STP0B]/ AN1/VREF	PA1	PAWU PAPU PASR	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	STP0B	PASR	—	CMOS	TM0 (STM) inverting output
	AN1	PASR	AN	—	ADC input channel 1
	VREF	PASR	AN	—	ADC VREF Input
PA2/[$\overline{\text{INT}}$]/ STP0/AN2/ VREFO	PA2	PAWU PAPU PASR	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	$\overline{\text{INT}}$	PASR IFS0	ST	—	External interrupt input
	STP0	PASR	—	CMOS	TM0 (STM) output
	AN2	PASR	AN	—	ADC input channel 2
	VREFO	PASR	—	AN	ADC reference voltage output
PA3/[$\overline{\text{INT}}$]	PA3	PAWU PAPU PASR	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	$\overline{\text{INT}}$	PASR IFS0	ST	—	External interrupt input
PA4	PA4	PAWU PAPU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PA5/$\overline{\text{INT}}$/ STP0B/AN3	PA5	PAWU PAPU PASR	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	$\overline{\text{INT}}$	PASR IFS0	ST	—	External interrupt input
	STP0B	PASR	—	CMOS	TM0 (STM) inverting output
	AN3	PASR	AN	—	ADC input channel 3
PA6/STP0I/ [STCK0]	PA6	PAWU PAPU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	STP0I	IFS0	ST	—	TM0 (STM) input
	STCK0	IFS0	ST	—	TM0 (STM) clock input

Pin Name	Function	OPT	I/T	O/T	Description
PA5/[$\overline{INT}$]/ PTP1I	PA5	PAWU PAPU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	$\overline{INT}$	PASR IFS0	ST	—	External interrupt input
	PTP1I	IFS0	ST	—	TM1 (PTM) input
PA6/[PTCK1]/ STP0I/[STP0]	PA6	PAWU PAPU PASR	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	PTCK1	PASR IFS0	ST	—	TM1 (PTM) clock input
	STP0I	PASR IFS0	ST	—	TM0 (STM) input
	STP0	PASR	—	CMOS	TM0 (STM) output
PA7/[PTCK1]/ [STP0B]/$\overline{RES}$	PA7	PAWU PAPU PASR	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	PTCK1	PASR IFS0	ST	—	TM1 (PTM) clock input
	STP0B	PASR	ST	CMOS	TM0 (STM) inverting output
	$\overline{RES}$	RSTC	ST	—	External reset input
PB0/[PTP1I]/ VREFO	PB0	PBPU PBSR	ST	CMOS	General purpose I/O. Register enabled pull-up
	PTP1I	PBSR IFS0	ST	—	TM1 (PTM) input
	VREFO	PBSR	—	AN	ADC reference voltage output
PB1/[PTCK1]/ STP0B	PB1	PBPU PBSR	ST	CMOS	General purpose I/O. Register enabled pull-up
	PTCK1	PBSR IFS0	ST	—	TM1 (PTM) clock input
	STP0B	PBSR	ST	CMOS	TM0 (STM) inverting output
PB2/PTP1B	PB2	PBPU PBSR	ST	CMOS	General purpose I/O. Register enabled pull-up
	PTP1B	PBSR	ST	CMOS	TM1 (PTM) inverting output
PB3/[PTP1]	PB3	PBPU PBSR	ST	CMOS	General purpose I/O. Register enabled pull-up
	PTP1	PBSR	—	CMOS	TM1 (PTM) output
PB4/[PTP1B]	PB4	PBPU PBSR	ST	CMOS	General purpose I/O. Register enabled pull-up
	PTP1B	PBSR	—	CMOS	TM1 (PTM) inverting output
PB5/PTP1	PB5	PBPU PBSR	ST	CMOS	General purpose I/O. Register enabled pull-up
	PTP1	PBSR	—	CMOS	TM1 (PTM) output
VDD	VDD	—	PWR	—	Digital positive power supply
AVDD	AVDD	—	PWR	—	Analog positive power supply
VSS	VSS	—	PWR	—	Digital negative power supply
AVSS	AVSS	—	PWR	—	Analog negative power supply

Pin Name	Function	OPT	I/T	O/T	Description
PB3/SCOM3/ AN7	PB3	PBPU PBSR	ST	CMOS	General purpose I/O. Register enabled pull-up
	SCOM3	SCOMC	—	SCOM	LCD driver output for LCD panel common
	AN7	PBSR	AN	—	ADC input channel 7
PB4/CLO/ SCOM2	PB4	PBPU PBSR	ST	CMOS	General purpose I/O. Register enabled pull-up
	CLO	PBSR	—	CMOS	System clock output
	SCOM2	SCOMC	—	SCOM	LCD driver output for LCD panel common
PB5/PTP0B	PB5	PBPU PBSR	ST	CMOS	General purpose I/O. Register enabled pull-up
	PTP0B	PBSR	ST	CMOS	PTM0 inverting output
PB6/PTP1B	PB6	PBPU PBSR	ST	CMOS	General purpose I/O. Register enabled pull-up
	PTP1B	PBSR	ST	CMOS	PTM1 inverting output
PC0/SCOM0	PC0	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	SCOM0	SCOMC	—	SCOM	LCD driver output for LCD panel common
PC1/SCOM1	PC1	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	SCOM1	SCOMC	—	SCOM	LCD driver output for LCD panel common
PC2/$\overline{RES}$	PC1	PCPU RSTC	ST	CMOS	General purpose I/O. Register enabled pull-up
	$\overline{RES}$	RSTC	ST	—	External reset input
VDD	VDD	—	PWR	—	Digital positive power supply
AVDD	AVDD	—	PWR	—	Analog positive power supply
VSS	VSS	—	PWR	—	Digital negative power supply
AVSS	AVSS	—	PWR	—	Analog negative power supply

Legend: I/T: Input type; O/T: Output type; PWR: Power;
OP: Optional by register option SCOM: Software controlled LCD COM
ST: Schmitt Trigger input; CMOS: CMOS output; AN: Analog pin
*: VDD is the device power supply while AVDD is the ADC power supply. The AVDD pin is bonded together internally with VDD.
**: VSS is the device ground pin while AVSS is the ADC ground pin. The AVSS pin is bonded together internally with VSS.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}−0.3V to V_{SS}+6.0V
Input Voltage ..... V_{SS}−0.3V to V_{DD}+0.3V
Storage Temperature..... -50˚C to 125˚C
Operating Temperature..... -40˚C to 85˚C
I_{OL} Total 80mA
I_{OH} Total ..... -80mA
Total Power Dissipation 500mW

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to these devices. Functional operation of these devices at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect devices reliability.

D.C. Characteristics

Ta = 25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage (HIRC)	—	f_{SYS}=8MHz	2.2	—	5.5	V
I_{DD1}	Operating Current, Normal Mode, $f_{SYS}=f_H$ (HIRC)	3V	No load, f_H=8MHz, ADC off, WDT enable, LVR enable	—	1.0	2.0	mA
		5V		—	2.0	3.0	mA
I_{DD2}	Operating Current, Slow Mode, $f_{SYS}=f_L$=LIRC	3V	No load, f_{SYS}=LIRC, ADC off, WDT enable , LVR enable	—	20	30	μA
		5V		—	30	60	μA
I_{DD3}	Operating Current, Normal Mode, f_H=8MHz (HIRC)	3V	No load, $f_{SYS}=f_H/2$, ADC off, WDT enable, LVR enable	—	1.0	1.5	mA
		5V		—	1.5	2.0	mA
		3V	No load, $f_{SYS}=f_H/4$, ADC off, WDT enable, LVR enable	—	0.9	1.3	mA
		5V		—	1.3	1.8	mA
		3V	No load, $f_{SYS}=f_H/8$, ADC off, WDT enable, LVR enable	—	0.8	1.1	mA
		5V		—	1.1	1.6	mA
		3V	No load, $f_{SYS}=f_H/16$, ADC off, WDT enable, LVR enable	—	0.7	1.0	mA
		5V		—	1.0	1.4	mA
		3V	No load, $f_{SYS}=f_H/32$, ADC off, WDT enable, LVR enable	—	0.6	0.9	mA
		5V		—	0.9	1.2	mA
		3V	No load, $f_{SYS}=f_H/64$, ADC off, WDT enable, LVR enable	—	0.5	0.8	mA
		5V		—	0.8	1.1	mA
I_{IDLE0}	IDLE0 Mode Standby Current (LIRC on)	3V	No load, ADC off, WDT enable, LVR disable	—	1.3	3.0	μA
		5V		—	5.0	10	μA
I_{IDLE1}	IDLE1 Mode Standby Current (HIRC)	3V	No load, ADC off, WDT enable, f_{SYS}=8MHz on	—	0.8	1.6	mA
		5V		—	1.0	2.0	mA
I_{SLEEP0}	SLEEP0 Mode Standby Current (LIRC off)	3V	No load, ADC off, WDT disable, LVR disable	—	0.1	1.0	μA
		5V		—	0.3	2.0	μA
I_{SLEEP1}	SLEEP1 Mode Standby Current (LIRC on)	3V	No load, ADC off, WDT enable, LVR disable	—	1.3	5.0	μA
		5V		—	2.2	10	μA
V_{IL1}	Input Low Voltage for I/O Ports or Input Pins except $\overline{RES}$ pin	5V	—	0	—	1.5	V
		—	—	0	—	$0.2V_{DD}$	V
V_{IH1}	Input High Voltage for I/O Ports or Input Pins except $\overline{RES}$ pin	5V	—	3.5	—	5.0	V
		—	—	$0.8V_{DD}$	—	V_{DD}	V
V_{IL2}	Input Low Voltage ($\overline{RES}$)	—	—	0	—	$0.4V_{DD}$	V
V_{IH2}	Input High Voltage ($\overline{RES}$)	—	—	$0.9V_{DD}$	—	V_{DD}	V
I_{OL}	I/O Port Sink Current	3V	$V_{OL}=0.1V_{DD}$	18	36	—	mA
		5V	$V_{OL}=0.1V_{DD}$	40	80	—	mA
I_{OH}	I/O Port, Source Current	3V	$V_{OH}=0.9V_{DD}$	-3	-6	—	mA
		5V	$V_{OH}=0.9V_{DD}$	-7	-14	—	mA
R_{PH}	Pull-high Resistance for I/O Ports	3V	—	20	60	100	kΩ
		5V	—	10	30	50	kΩ
I_{OCDS}	Operating Current, Normal Mode, $f_{SYS}=f_H$ (HIRC) (for OCDS EV testing, connect to an e-Link)	3V	No load, f_H=8MHz, ADC off, WDT enable	—	1.4	2.0	mA

A.C. Characteristics

Ta = 25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
f_{CPU}	Operating Clock	2.2~5.5V	—	DC	—	8	MHz
f_{HIRC}	System Clock (HIRC)	3V/5V	Ta = 25°C	-2%	8	+2%	MHz
		3V/5V	Ta = 0°C to 70°C	-5%	8	+5%	MHz
		2.2V~5.5V	Ta = 0°C to 70°C	-8%	8	+8%	MHz
		2.2V~5.5V	Ta = -40°C to 85°C	-12%	8	+12%	MHz
f_{LIRC}	System Clock (LIRC)	2.2V~5.5V	Ta = -40°C to 85°C	8	32	50	kHz
t_{TIMER}	xTCKn, xTPnI Input Pulse Width	—	—	0.3	—	—	μs
t_{RES}	External Reset Low Pulse Width	—	—	10	—	—	μs
t_{INT}	Interrupt Pulse Width	—	—	0.3	—	—	μs
t_{EERD}	EEPROM Read Time	—	—	—	2	4	t_{SYS}
t_{EEWR}	EEPROM Write Time	—	—	—	2	5	ms
t_{SST}	System Start-up Timer Period (Wake-up from HALT, f_{SYS} off at HALT state)	—	f_{SYS} =HIRC	16	—	—	t_{SYS}
			f_{SYS} =LIRC	2	—	—	
t_{RSTD}	System Reset Delay Time (Power On Reset, LVR reset, WDT S/W reset(WDTC)	—	—	25	50	100	ms
	System Reset Delay Time (RES reset, WDT normal reset)	—	—	8.3	16.7	33.3	ms

Note: 1. $t_{SYS}= 1/f_{SYS}$

2. To maintain the accuracy of the internal HIRC oscillator frequency, a 0.1μF decoupling capacitor should be connected between VDD and VSS and located as close to the device as possible.

ADC Electrical Characteristics

Ta = 25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
AV_{DD}	A/D Converter Operating Voltage	—	—	2.7	—	5.5	V
V_{ADI}	A/D Converter Input Voltage	—	—	0	—	AV_{DD} / V_{REF}	V
V_{REF}	A/D Converter Reference Voltage	3V	—	2	—	AV_{DD}	V
		5V					
DNL	Differential Non-linearity	2.7V	$V_{REF}=AV_{DD}=V_{DD}$ t_{ADCK} =0.5μs	-3	—	+3	LSB
		3V					
		5V					
INL	Integral Non-linearity	2.7V	$V_{REF}=AV_{DD}=V_{DD}$ t_{ADCK} =0.5μs	-4	—	+4	LSB
		3V					
		5V					
I_{ADC}	Additional Power Consumption if A/D Converter is used	3V	No load (t_{ADCK} =0.5μs)	—	1.0	2.0	mA
		5V	No load (t_{ADCK} =0.5μs)	—	1.5	3.0	mA
t_{ADCK}	A/D Converter Clock Period	2.7~ 5.5V	—	0.5	—	10	μs
t_{ADC}	A/D Conversion Time (Include Sample and Hold Time)	2.7~ 5.5V	12-bit ADC	16	—	20	t_{ADCK}
t_{ADS}	A/D Converter Sampling Time	2.7~ 5.5V	—	—	4	—	t_{ADCK}
t_{ON2ST}	A/D Converter On-to-Start Time	2.7~ 5.5V	—	4	—	—	μs

OPA Electrical Characteristics

Ta = 25°C

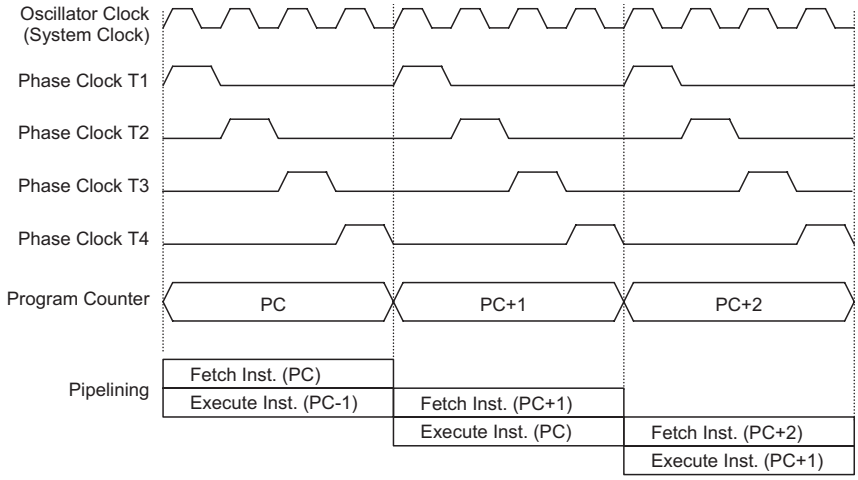
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
AV_{DD}	OPA operating voltage	—	—	2.7	—	5.5	V
I_{OPA}	OPA operating current	5V	No load	—	200	350	μA
V_{OPOS1}	Input offset voltage	5V	—	-15	—	15	mV
V_{CM}	Common mode voltage range	5V	—	0.2	—	V_{DD}-4	V
PSRR	Power Supply Rejection Ratio	5V	—	60	80	—	dB
CMRR	Common mode Rejection Ratio	5V	—	60	80	—	dB
SR	Slew rate +, Slew rate -	5V	—	0.8	1.5	—	V/μs
GBW	Gain Band Width	5V	—	500	—	—	kHz
ERRG	OPA gain error	5V	Gain=1/2/3/4 If OPA input voltage ≥ 0.2V	-5	Gain	+5	%

System Architecture

A key factor in the high-performance features of the Holtek range of microcontrollers is attributed to their internal system architecture. The device takes advantage of the usual features found within RISC microcontrollers providing increased speed of operation and Periodic performance. The pipelining scheme is implemented in such a way that instruction fetching and instruction execution are overlapped, hence instructions are effectively executed in one cycle, with the exception of branch or call instructions. An 8-bit wide ALU is used in practically all instruction set operations, which carries out arithmetic operations, logic operations, rotation, increment, decrement, branch decisions, etc. The internal data path is simplified by moving data through the Accumulator and the ALU. Certain internal registers are implemented in the Data Memory and can be directly or indirectly addressed. The simple addressing methods of these registers along with additional architectural features ensure that a minimum of external components is required to provide a functional I/O and A/D control system with maximum reliability and flexibility. This makes these devices suitable for low-cost, high-volume production for controller applications

Clocking and Pipelining

The main system clock, derived from either a HIRC or LIRC oscillator is subdivided into four internally generated non-overlapping clocks, T1~T4. The Program Counter is incremented at the beginning of the T1 clock during which time a new instruction is fetched. The remaining T2~T4 clocks carry out the decoding and execution functions. In this way, one T1~T4 clock cycle forms one instruction cycle. Although the fetching and execution of instructions takes place in consecutive instruction cycles, the pipelining structure of the microcontroller ensures that instructions are effectively executed in one instruction cycle. The exception to this are instructions where the contents of the Program Counter are changed, such as subroutine calls or jumps, in which case the instruction will take one more instruction cycle to execute.



System Clock and Pipelining

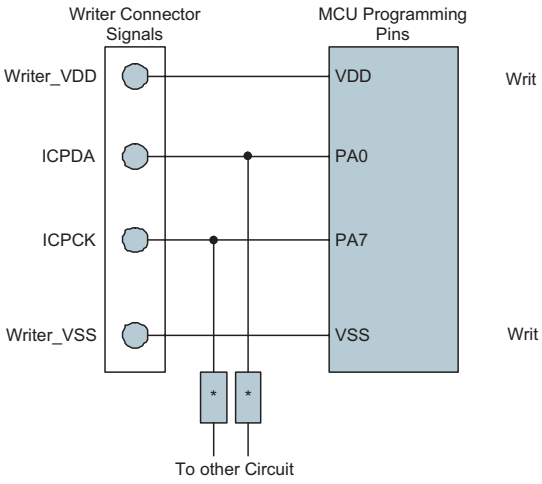
For instructions involving branches, such as jump or call instructions, two machine cycles are required to complete instruction execution. An extra cycle is required as the program takes one cycle to first obtain the actual jump or call address and then another cycle to actually execute the branch. The requirement for this extra cycle should be taken into account by programmers in timing sensitive applications.

In Circuit Programming

The provision of Flash type Program Memory provides the user with a means of convenient and easy upgrades and modifications to their programs on the same device. As an additional convenience, Holtek has provided a means of programming the microcontroller in-circuit using a 4-pin interface. This provides manufacturers with the possibility of manufacturing their circuit boards complete with a programmed or un-programmed microcontroller, and then programming or upgrading the program at a later stage. This enables product manufacturers to easily keep their manufactured products supplied with the latest program releases without removal and re-insertion of the device.

Holtek Write Pins	MCU Programming Pins		Function
	JXY-FC08		
ICPDA	PA0		Programming Serial Data
ICPCK	PA7	PA2	Programming Serial Clock
VDD	VDD		Power Supply
VSS	VSS		Ground

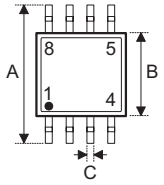
The Program Memory and EEPROM data memory can both be programmed serially in-circuit using this 4-wire interface. Data is downloaded and uploaded serially on a single pin with an additional line for the clock. Two additional lines are required for the power supply and ground. The technical details regarding the in-circuit programming of the device are beyond the scope of this document and will be supplied in supplementary literature.

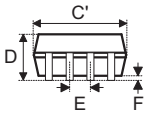


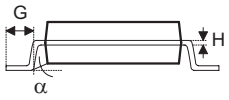
JXY-FC08

Note: * may be resistor or capacitor. The resistance of * must be greater than 1k or the capacitance of * must be less than 1nF.

8-pin SOP (150mil) Outline Dimensions



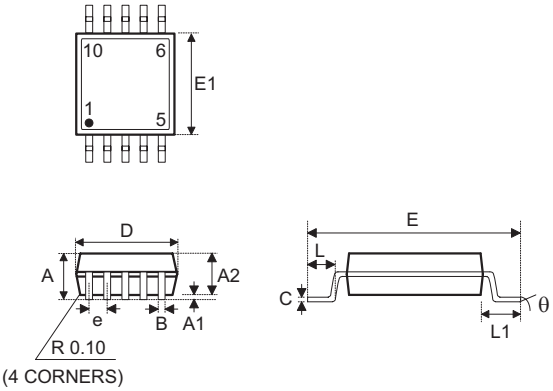




Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C’	—	0.193 BSC	—
D	—	—	0.069
E	—	0.050 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.31	—	0.51
C’	—	4.90 BSC	—
D	—	—	1.75
E	—	1.27 BSC	—
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

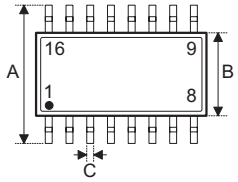
10-pin MSOP Outline Dimensions

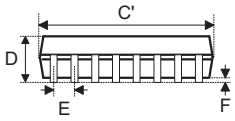


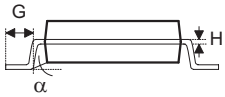
Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	—	0.043
A1	0.000	—	0.006
A2	0.030	0.033	0.037
B	0.007	—	0.013
C	0.003	—	0.009
D	—	0.118 BSC	—
E	—	0.193 BSC	—
E1	—	0.118 BSC	—
e	—	0.020 BSC	—
L	0.016	0.024	0.031
L1	—	0.037 BSC	—
y	—	0.004	—
θ	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	0.85	0.95
B	0.17	—	0.33
C	0.08	—	0.23
D	—	3.0 BSC	—
E	—	4.9 BSC	—
E1	—	3.0 BSC	—
e	—	0.5 BSC	—
L	0.40	0.60	0.80
L1	—	0.95 BSC	—
y	—	0.1	—
θ	0°	—	8°

16-pin NSOP (150mil) Outline Dimensions







Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C’	—	0.390 BSC	—
D	—	—	0.069
E	—	0.050 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.0 BSC	—
B	—	3.9 BSC	—
C	0.31	—	0.51
C’	—	9.9 BSC	—
D	—	—	1.75
E	—	1.27 BSC	—
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

20-pin DIP (300mil) Outline Dimensions

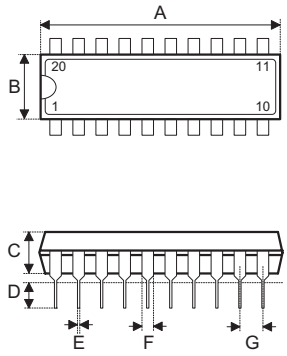


Fig 1. Full Lead Packages

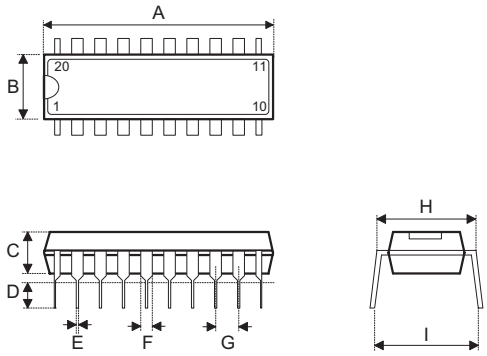


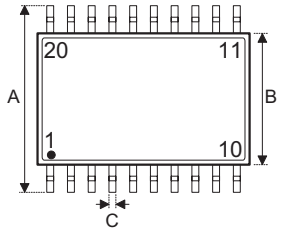
Fig 2. 1/2 Lead Packages

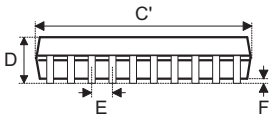
See Fig 1

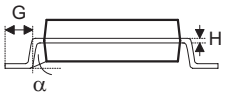
Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.980	1.030	1.060
B	0.240	0.250	0.280
C	0.115	0.130	0.195
D	0.115	0.130	0.150
E	0.014	0.018	0.022
F	0.045	0.060	0.070
G	—	0.1BSC	—
H	0.300	0.310	0.325
I	—	—	0.430

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	24.89	26.16	26.92
B	6.10	6.35	7.11
C	2.92	3.30	4.95
D	2.92	3.30	3.81
E	0.36	0.46	0.56
F	1.14	1.52	1.78
G	—	2.54 BSC	—
H	7.62	7.87	8.26
I	—	—	10.92

20-pin SOP (300mil) Outline Dimensions



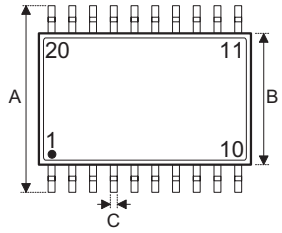


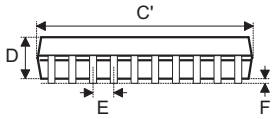


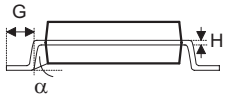
Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.406 BSC	—
B	—	0.406 BSC	—
C	0.012	—	0.020
C’	—	0.504 BSC	—
D	—	—	0.104
E	—	0.050 BSC	—
F	0.004	—	0.012
G	0.016	—	0.050
H	0.008	—	0.013
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	10.30 BSC	—
B	—	7.50 BSC	—
C	—	7.50 BSC	—
C’	—	12.80 BSC	—
D	—	12.80 BSC	—
E	—	1.27 BSC	—
F	0.10	—	0.30
G	0.40	—	1.27
H	0.40	—	1.27
α	0°	—	8°

20-pin SSOP (150mil) Outline Dimensions







Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.155 BSC	—
C	0.008	—	0.012
C’	—	0.341 BSC	—
D	—	—	0.069
E	—	0.025 BSC	—
F	0.004	—	0.0098
G	0.016	—	0.05
H	0.004	—	0.01
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.20	—	0.30
C‘	—	8.66 BSC	—
D	—	—	1.75
E	—	0.635 BSC	—
F	0.10	—	0.25
G	0.41	—	1.27
H	0.10	—	0.25
α	0°	—	8°