JXY-FC40HV

Power Bank Flash MCU

深圳市集芯源电子科技有限公司

www.szjixinyuan.com

Features

CPU Features

- Operating voltage
  - f_{SYS}=8MHz: 2.2V~5.5V
  - f_{SYS}=12MHz: 2.7V~5.5V
  - f_{SYS}=16MHz: 3.3V~5.5V
- Up to 0.25μs instruction cycle with 16MHz system clock at V_{DD}=5V
- Power down and wake-up functions to reduce power consumption
- Oscillator types
  - Internal High Speed RC – HIRC
  - Internal Low Speed 32kHz RC – LIRC
- Multi-mode operation: FAST, SLOW, IDLE and SLEEP
- Fully integrated internal oscillators require no external components
- All instructions executed in 1~3 instruction cycles
- Table read instructions
- 115 powerful instructions
- 8-level subroutine nesting
- Bit manipulation instruction

Peripheral Features

- Flash Program Memory: 6K×16
- Data Memory: 256×8
- True EEPROM Memory: 64×8
- Watchdog Timer function
- 28 bidirectional I/O lines
- 8 bidirectional High Voltage output lines with short-circuit protection function
- Three pin-shared external interrupts
- Multiple Timer Modules for time measurement, input capture, compare match output or PWM output or single pulse output function
  - Single standard type 16-bit Timer Module – STM
  - Single periodic type 10-bit Timer Module – PTM
- Auto Adjust High Resolution PWM with Delay Lock Loop/Dead-Time
- Two over current protection (OCP) with interrupts
- Two sets of Over/Under voltage protection (OUVP) with interrupts
- USB auto detection function
- Dual Time-Base functions for generation of fixed time interrupt signals
- Multi-channel 12-bit resolution A/D converter with a Programmable Reference Voltage V_R
- Low voltage reset function
- Low voltage detect function
- Integrated Low Dropout Voltage Regulator – LDO
- Package type: 46-pin QFN

General Description

The device is a Flash Memory A/D type 8-bit high performance RISC architecture microcontroller, specifically designed for Power Bank applications. Offering users the convenience of Flash Memory multi-programming features, the device also includes a wide range of functions and features. Other memory includes an area of RAM Data Memory as well as an area of true EEPROM memory for storage of non-volatile data such as serial numbers, calibration data etc.

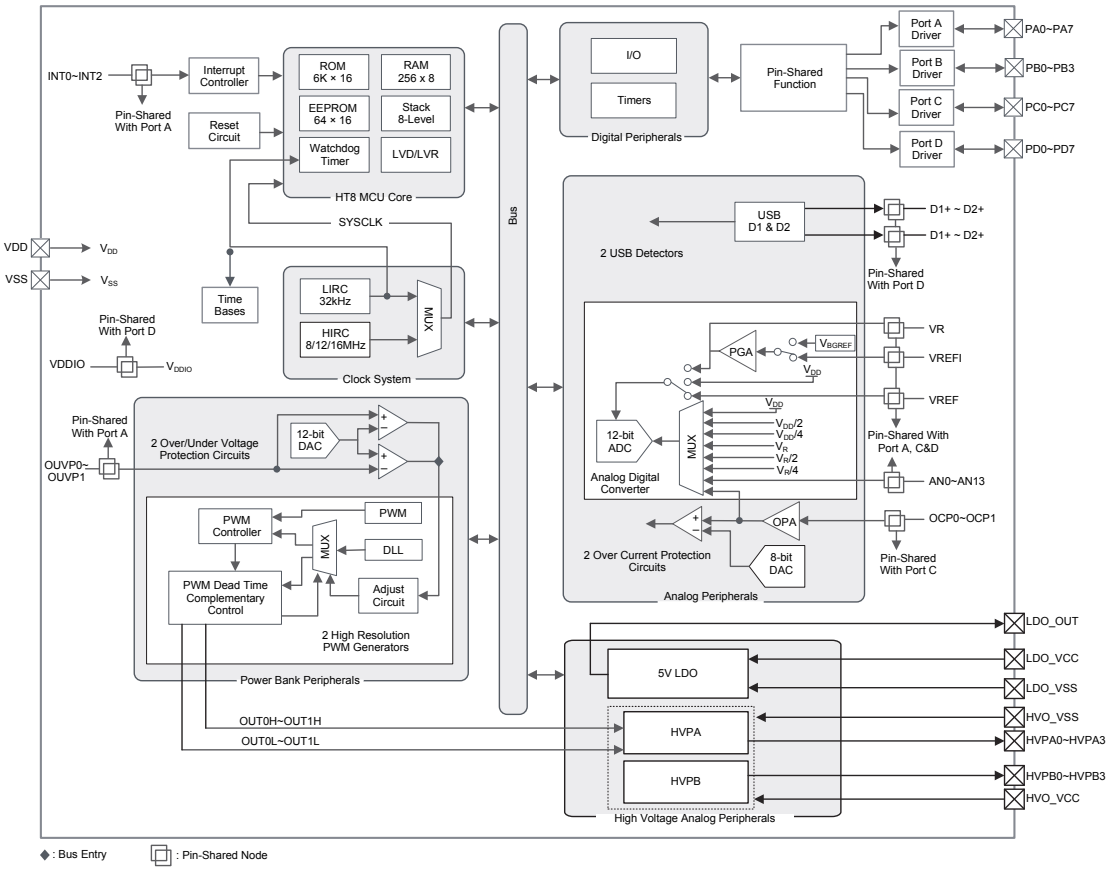
Analog features include a multi-channel 12-bit A/D converter and an internal 5V LDO (Low Dropout Regulator) for voltage regulator, two over current protection functions, two sets of over/under voltage protection functions, Auto Adjust High Resolution PWM with Delay Lock Loop/Dead-Time function and an USB device auto detection function. Multiple and extremely flexible Timer Modules provide timing, pulse generation and PWM generation functions. Protective features such as an internal Watchdog Timer, Low Voltage Reset and Low Voltage Detector coupled with excellent noise immunity and ESD protection ensure that reliable operation is maintained in hostile electrical environments.

The device also includes fully integrated high and low speed oscillators which require no external components for their implementation. The ability to operate and switch dynamically between a range of operating modes using different clock sources gives users the ability to optimize microcontroller operation and minimize power consumption.

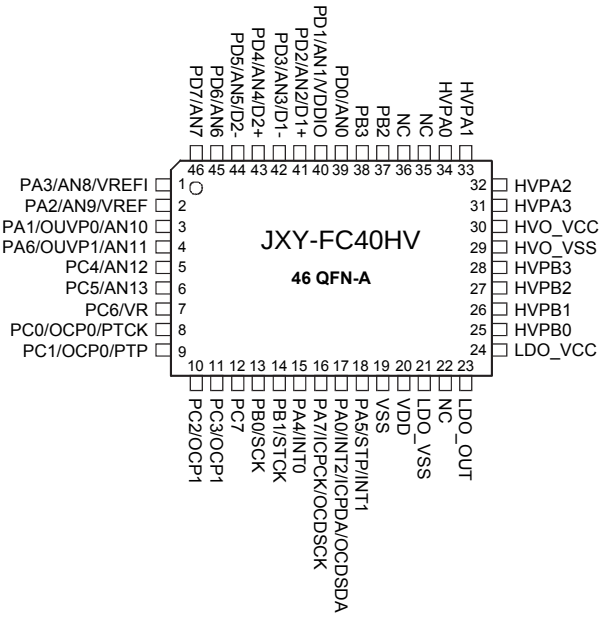
The High Voltage Output function specific to high voltage and high current applications is also fully integrated within the device. The inclusion of flexible I/O programming features, Time-Base functions along with many other features ensure that the device will find excellent use in different power bank applications.

Circuitry specific to Power Bank applications is also fully integrated within the device. These include functions such as over and under voltage protection, over current protection and auto detect. These features combine to ensure that a minimum of external components is required to implement Power Bank applications, providing the benefits of reduced component count and reduced circuit board areas.

Block Diagram



Pin Assignment



Note: 1. If the pin-shared pin functions have multiple outputs simultaneously, the desired pin-shared function is determined by the corresponding software control bits.

2. The OCDSDA and OCDSCK pins are supplied for the OCDS dedicated pins and as such only available for the JXY-FC40HV device which is the OCDS EVchip for the JXY-FC40HV device

Pin Description

With the exception of the power pins and some relevant transformer control pins, all pins on the device can be referenced by their Port name, e.g. PA0, PA1 etc., which refer to the digital I/O function of the pins. However these Port pins are also shared with other function such as the Analog to Digital Converter, Timer Module pins etc. The function of each pin is listed in the following table, however the details behind how each pin is configured is contained in other sections of the datasheet.

Pin Name	Function	OPT	I/T	O/T	Descriptions
PA0/INT2/ ICPDA/OCDSDA	PA0	PAWU PAPU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	INT2	INTEG INTC0	ST	—	External interrupt 2 input
	ICPDA	—	ST	CMOS	In-circuit programming data/address pin
	OCDSDA	—	ST	CMOS	On-chip debug support data/address pin- for EV chip only
PA1/OUVP0/ AN10	PA1	PAWU PAPU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	OUVP0	PAS0	AN	—	OVP/UVP 0 input
	AN10	PAS0	AN	—	A/D converter external signal input channel 10
PA2/AN9/VREF	PA2	PAWU PAPU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN9	PAS0	AN	—	A/D converter external signal input channel 9
	VREF	PAS0	AN	—	A/D converter and OVPn/OUVPn D/A converter external reference input

Pin Name	Function	OPT	I/T	O/T	Descriptions
PA3/AN8/VREFI	PA3	PAWU PAPU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN8	PAS0	AN	—	A/D converter external signal input channel 8
	VREFI	PAS0	AN	—	A/D converter external reference voltage input
PA4/INT0	PA4	PAWU PAPU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	INT0	PAS1 INTEG INTC0	ST	—	External interrupt 0 input
PA5/STP/INT1	PA5	PAWU PAPU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	STP	PAS1	ST	CMOS	STM output or STM capture input
	INT1	PAS1 INTEG INTC0	ST	—	External interrupt 1 input
PA6/OUVP1/ AN11	PA6	PAWU PAPU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	OUVP1	PAS1	AN	—	OVP/UVP 1 input
	AN11	PAS1	AN	—	A/D converter external signal input channel 11
PA7/ICPCK/ OCDSCK	PA7	PAWU PAPU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	ICPCK	—	ST	—	ICP clock input
	OCDSCK	—	ST	—	OCDS clock input- for EV chip only.
PB0	PB0	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up
PB1/STCK	PB1	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	STCK	—	ST	—	STM input
PB2~PB3	PB2~PB3	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up
PC0/OCP0/ PTCK	PC0	PCPU PCS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	OCP0	PCS0	AN	—	OCP0 input
	PTCK	PCS0	ST	—	PTM input
PC1/OCP0/PTP	PC1	PCPU PCS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	OCP0	PCS0	AN	—	OCP0 input
	PTP	PCS0	ST	CMOS	PTM output or PTM capture input
PC2/OCP1	PC2	PCPU PCS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	OCP1	PCS0	AN	—	General purpose I/O. Register enabled pull-up
PC3/OCP1	PC3	PCPU PCS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	OCP1	PCS0	AN	—	OCP1 input
PC4/AN12	PC4	PCPU PCS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN12	PCS1	AN	—	A/D converter external signal input channel 12
PC5/AN13	PC5	PCPU PCS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN13	PCS1	AN	—	A/D converter external signal input channel 13

Pin Name	Function	OPT	I/T	O/T	Descriptions
PC6/VR	PC6	PCPU PCS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	VR	PCS1	—	AN	A/D converter external reference voltage output
PC7	PC7	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
PD0/AN0	PD0	PDPU PDS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN0	PDS0	AN	—	A/D converter external signal input channel 0
PD1/AN1/VDDIO	PD1	PDPU PDS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN1	PDS0	AN	—	A/D converter external signal input channel 1
	VDDIO	PDS0	PWR	—	Power supply for PD2~PD5 input/output pins
PD2/AN2/D1+	PD2	PDPU PDS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN2	PDS0	AN	—	A/D converter external signal input channel 2
	D1+	PDS0	—	AN	USB DAC0 output pin
PD3/AN3/D1-	PD3	PDPU PDS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN3	PDS0	AN	—	A/D converter external signal input channel 3
	D1-	PDS0	—	AN	USB DAC1 output pin
PD4/AN4/D2+	PD4	PDPU PDS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN4	PDS1	AN	—	A/D converter external signal input channel 4
	D2+	PDS1	–	AN	USB DAC2 output pin
PD5/AN5/D2-	PD5	PDPU PDS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN5	PDS1	AN	—	A/D converter external signal input channel 5
	D2-	PDS1	—	AN	USB DAC3 output pin
PD6/AN6	PD6	PDPU PDS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN6	PDS1	AN	—	A/D converter external signal input channel 6
PD7/AN7	PD7	PDPU PDS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN7	PDS1	AN	—	A/D converter external signal input channel 7
HVPA0~HVPA3	HVPA0~ HVPA3	HVPAEN	—	AN	High voltage Output
HVPB0~HVPB3	HVPB0~ HVPB3	HVPBEN	—	AN	High voltage Output
VDD	VDD	—	PWR	—	Digital positive power supply
VSS	VSS	—	PWR	—	Digital negative power supply, ground
HVO_VCC	HVO_ VCC	—	PWR	—	HVO and Level Shifter High voltage power supply
HVO_VSS	HVO_VSS	—	PWR	—	High voltage negative power supply, ground
LDO_OUT	LDO_OUT	—	—	PWR	LDO output voltage
LDO_VCC	LDO_VCC	—	PWR	—	LDO High voltage power supply
LDO_VSS	LDO_VSS	—	PWR	—	LDO negative power supply, ground

Legend: I/T: Input type; O/T: Output type;
OPT: Optional by register option; PWR: Power;
ST: Schmitt Trigger input; CMOS: CMOS output;
AN: Analog signal.

Absolute Maximum Ratings

Supply Voltage (V_{LDO_VCC}, V_{HVO_VCC}) ..... V_{SS}-0.3V to 13.5V

Supply Voltage (V_{DD}) ..... V_{SS}-0.3V to 6.0V

High Voltage Input Voltage ..... V_{SS}-0.3V to V_{HVO_VCC}+0.3V

Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature ..... -50˚C to 125˚C

Operating Temperature ..... -40˚C to 85˚C

I_{OH} Total ..... -120mA

I_{OL} Total 120mA

Total Power Dissipation 600mW

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of the device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

For data in the following tables, note that factors such as oscillator type, operating voltage, operating frequency, pin load conditions, temperature and program instruction type, etc., can all exert an influence on the measured values.

Operating Voltage Characteristics

Ta=-40˚C~85˚C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage – HIRC	f_{SYS}=f_{HIRC}=8MHz	2.2	—	5.5	V
		f_{SYS}=f_{HIRC}=12MHz	2.7	—	5.5	
		f_{SYS}=f_{HIRC}=16MHz	3.3	—	5.5	
	Operating Voltage – LIRC	f_{SYS}=f_{LIRC}=32kHz	V_{LVR}	—	5.5	V
V_{DDIO}	VDDIO Power Supply for PD2~PD5 Pins	—	1.8	—	V_{DD}	V

A.C. Characteristics

For data in the following tables, note that factors such as oscillator type, operating voltage, operating frequency and temperature etc., can all exert an influence on the measured values.

High Speed Internal Oscillator – HIRC – Frequency Accuracy

During the program writing operation the writer will trim the HIRC oscillator at a user selected HIRC frequency and user selected voltage of either 3V or 5V.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Temp.				
f_{HIRC}	8MHz Writer Trimmed HIRC Frequency	3V/5V	25˚C	-1%	8	+1%	MHz
			-40˚C~85˚C	-2%	8	+2%	
		2.2V~5.5V	25˚C	-2.5%	8	+2.5%	
			-40˚C~85˚C	-3%	8	+3%	
	12MHz Writer Trimmed HIRC Frequency	3V/5V	25˚C	-1%	12	+1%	MHz
			-40˚C~85˚C	-2%	12	+2%	
		2.7V~5.5V	25˚C	-2.5%	12	+2.5%	
			-40˚C~85˚C	-3%	12	+3%	
	16MHz Writer Trimmed HIRC Frequency	5V	25˚C	-1%	16	+1%	MHz
			-40˚C~85˚C	-2%	16	+2%	
		3.3V~5.5V	25˚C	-2.5%	16	+2.5%	
			-40˚C~85˚C	-3%	16	+3%	

Note: 1. The 3V/5V values for V_{DD} are provided as these are the two selectable fixed voltages at which the HIRC frequency is trimmed by the writer.

2. The row below the 3V/5V trim voltage row is provided to show the values for the full V_{DD} range operating voltage. It is recommended that the trim voltage is fixed at 3V for application voltage ranges from 2.2 to 3.6V and fixed at 5V for application voltage ranges from 3.3V to 5.5V.

3. The minimum and maximum tolerance values provided in the table are only for the frequency at which the writer trims the HIRC oscillator. After trimming at this chosen specific frequency any change in HIRC oscillator frequency using the oscillator register control bits by the application program will give a frequency tolerance to within ±20%.

Low Speed Internal Oscillator Characteristics – LIRC

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Temp.				
f_{LIRC}	Oscillator Frequency	5V	25˚C	-10%	32	+10%	kHz
		5V±0.5V	-40˚C~85˚C	-40%	32	+40%	
		V_{LVR}~5.5V	-40˚C~85˚C	-50%	32	+60%	

Input/Output Characteristics

Input/Output (without Multi-power) D.C. Characteristics

Ta=25˚C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IL}	Input Low Voltage for I/O Ports except PD2~PD5 Pins	5V	—	0	—	1.5	V
		—	—	0	—	$0.2V_{DD}$	
V_{IH}	Input High Voltage for I/O Ports except PD2~PD5 Pins	5V	—	3.5	—	5.0	V
		—	—	$0.8V_{DD}$	—	V_{DD}	
I_{OL}	Sink Current for I/O Ports except PD2~PD5 Pins	3V	$V_{OL}=0.1V_{DD}$	16	32	—	mA
		5V		32	65	—	
I_{OH}	Source Current for I/O Ports except PD2~PD5 Pins	3V	$V_{OH}=0.9V_{DD}$	-4	-8	—	mA
		5V		-8	-16	—	
R_{PH}	Pull-high Resistance for I/O Ports except PD2~PD5 Pins (Note)	3V	—	20	60	100	kΩ
		5V	—	10	30	50	
t_{TCK}	PTCK and STCK Clock Input Minimum Pulse Width	—	—	0.3	—	—	μs
t_{INT}	Interrupt Input Pin Minimum Pulse Width	—	—	10	—	—	μs

Input/Output (with Multi-power) D.C. Characteristics

Ta=25˚C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	VDD Power Supply for PD2~PD5 Pins	—	—	2.2	5	5.5	V
V_{DDIO}	VDDIO Power Supply for PD2~PD5 Pins	—	—	1.8	—	V_{DD}	V
V_{IL}	Input Low Voltage for PD2~PD5 Pins	5V	—	0	—	1.5	V
		—	Pin power=V_{DD} or V_{DDIO}	0	—	0.2 (V_{DD} or V_{DDIO})	
V_{IH}	Input High Voltage for PD2~PD5 Pins	5V	—	3.5	—	5.0	V
		—	Pin power=V_{DD} or V_{DDIO}	$0.8V_{DD}$	—	V_{DD} or V_{DDIO}	
I_{OL}	Sink Current for PD2~PD5 Pins	3V	$V_{OL}=0.1(V_{DD}$ or $V_{DDIO})$, $V_{DDIO}=V_{DD}$	16	32	—	mA
		5V	$V_{OL}=0.1(V_{DD}$ or $V_{DDIO})$, $V_{DDIO}=V_{DD}$	32	65	—	
			$V_{OL}=0.1(V_{DD}$ or $V_{DDIO})$, $V_{DDIO}=3V$	20	40	—	
I_{OH}	Source Current for PD2~PD5 Pins	3V	$V_{OH}=0.9(V_{DD}$ or $V_{DDIO})$, $V_{DDIO}=V_{DD}$	-4	-8	—	mA
		5V	$V_{OH}=0.9(V_{DD}$ or $V_{DDIO})$, $V_{DDIO}=V_{DD}$	-8	-16	—	
			$V_{OH}=0.9(V_{DD}$ or $V_{DDIO})$, $V_{DDIO}=3V$	-2.5	-5	—	
R_{PH}	Pull-high Resistance for PD2~PD5 Pins (Note)	3V	$V_{DDIO}=V_{DD}$, LVPU=0, PDPU5~2=1	20	60	100	kΩ
		5V	$V_{DDIO}=V_{DD}$, LVPU=0, PDPU5~2=1	10	30	50	
		3V	$V_{DDIO}=V_{DD}$, LVPU=1, PDPU5~2=1	6.67	15	23	
		5V	$V_{DDIO}=V_{DD}$, LVPU=1, PDPU5~2=1	3.5	7.5	12	
I_{LEAK}	Input Leakage Current for PD2~PD5 Pins	5V	$V_{IN}=V_{DD}$ or $V_{IN}=V_{DDIO}$ or $V_{IN}=V_{SS}$	—	—	±1	μA

Note: The R_{PH} internal pull high resistance value is calculated by connecting to ground and enabling the input pin with a pull-high resistor and then measuring pin current at the specified supply voltage level. Dividing the voltage by this measured current provides the R_{PH} value.

Memory Characteristics

Ta=-40˚C~85˚C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{RW}	V_{DD} for Read/Write	—	—	V_{DDmin}	—	V_{DDmax}	V
Flash Program/Data EEPROM Memory							
t_{DEW}	Erase/Write Time – Flash Program Memory	—	—	—	2	3	ms
	Write Cycle Time – Data EEPROM Memory	—	—	—	4	6	ms
I_{DDPGM}	Programming/Erase current on V_{DD}	—	—	—	—	5.0	mA
E_P	Cell Endurance	—	—	100K	—	—	E/W
t_{RETD}	ROM Data Retention time	—	Ta=25˚C	—	40	—	Year
RAM Data Memory							
V_{DR}	RAM Data Retention voltage	—	Device in SLEEP Mode	1.0	—	—	V

LVD/LVR Electrical Characteristics

Ta=-40˚C~85˚C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{LVR}	Low Voltage Reset Voltage	—	LVR enable	-5%	2.55	+5%	V
V_{LVD}	Low Voltage Detection Voltage	—	LVD enable, voltage select 2.7V	-5%	2.7	+5%	V
		—	LVD enable, voltage select 3.0V		3.0		
		—	LVD enable, voltage select 3.3V		3.3		
		—	LVD enable, voltage select 3.6V		3.6		
		—	LVD enable, voltage select 4.0V		4.0		
V_{BG}	Bandgap reference voltage	—	Trim @ V_{DD}=3.15V	-5%	1.25	+5%	V
I_{LVR}	Additional Current for LVR Enable	—	LVD disable	—	—	10	μA
I_{LVD}	Additional Current for LVD Enable	—	LVR disable	—	60	90	μA
t_{LVDS}	LVDO Stable Time	—	For LVR enable, LVD off → on	—	—	15	μs
t_{BGS}	V_{BG} turn on stable time	—	No load	—	—	150	μs
t_{LVR}	Minimum Low Voltage Width to Reset	—	—	120	240	480	μs
t_{LVD}	Minimum Low Voltage Width to Interrupt	—	—	60	120	240	μs

Note: The V_{BG} voltage is used as the A/D converter internal signal input.

A/D Converter Electrical Characteristics

Ta=-40˚C~85˚C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.2	—	5.5	V
V_{ADI}	Input Voltage	—	—	0	—	V_{REF}	V
V_{REF}	Reference Voltage	—	—	2	—	V_{DD}	V
DNL	Differential Non-linearity	3V	SAINS[3:0]=0000B, SAVRS[1:0]=01B, V_{REF}=V_{DD}, t_{ADCK}=0.5μs	-3	—	+3	LSB
		5V					
		3V	SAINS[3:0]=0000B, SAVRS[1:0]=01B, V_{REF}=V_{DD}, t_{ADCK}=10μs				
		5V					

Input/Output Characteristics

Input/Output (without Multi-power) D.C. Characteristics

Ta=25˚C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IL}	Input Low Voltage for I/O Ports except PD2~PD5 Pins	5V	—	0	—	1.5	V
		—	—	0	—	$0.2V_{DD}$	
V_{IH}	Input High Voltage for I/O Ports except PD2~PD5 Pins	5V	—	3.5	—	5.0	V
		—	—	$0.8V_{DD}$	—	V_{DD}	
I_{OL}	Sink Current for I/O Ports except PD2~PD5 Pins	3V	$V_{OL}=0.1V_{DD}$	16	32	—	mA
		5V		32	65	—	
I_{OH}	Source Current for I/O Ports except PD2~PD5 Pins	3V	$V_{OH}=0.9V_{DD}$	-4	-8	—	mA
		5V		-8	-16	—	
R_{PH}	Pull-high Resistance for I/O Ports except PD2~PD5 Pins (Note)	3V	—	20	60	100	kΩ
		5V	—	10	30	50	
t_{TCK}	PTCK and STCK Clock Input Minimum Pulse Width	—	—	0.3	—	—	μs
t_{INT}	Interrupt Input Pin Minimum Pulse Width	—	—	10	—	—	μs

Input/Output (with Multi-power) D.C. Characteristics

Ta=25˚C

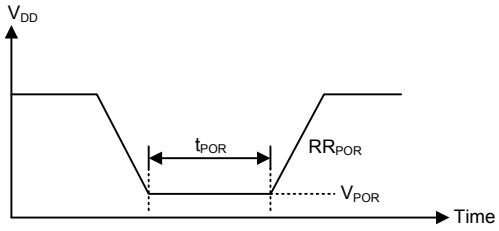
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	VDD Power Supply for PD2~PD5 Pins	—	—	2.2	5	5.5	V
V_{DDIO}	VDDIO Power Supply for PD2~PD5 Pins	—	—	1.8	—	V_{DD}	V
V_{IL}	Input Low Voltage for PD2~PD5 Pins	5V	—	0	—	1.5	V
		—	Pin power=V_{DD} or V_{DDIO}	0	—	0.2 (V_{DD} or V_{DDIO})	
V_{IH}	Input High Voltage for PD2~PD5 Pins	5V	—	3.5	—	5.0	V
		—	Pin power=V_{DD} or V_{DDIO}	$0.8V_{DD}$	—	V_{DD} or V_{DDIO}	
I_{OL}	Sink Current for PD2~PD5 Pins	3V	$V_{OL}=0.1(V_{DD}$ or $V_{DDIO})$, $V_{DDIO}=V_{DD}$	16	32	—	mA
		5V	$V_{OL}=0.1(V_{DD}$ or $V_{DDIO})$, $V_{DDIO}=V_{DD}$	32	65	—	
			$V_{OL}=0.1(V_{DD}$ or $V_{DDIO})$, $V_{DDIO}=3V$	20	40	—	
I_{OH}	Source Current for PD2~PD5 Pins	3V	$V_{OH}=0.9(V_{DD}$ or $V_{DDIO})$, $V_{DDIO}=V_{DD}$	-4	-8	—	mA
		5V	$V_{OH}=0.9(V_{DD}$ or $V_{DDIO})$, $V_{DDIO}=V_{DD}$	-8	-16	—	
			$V_{OH}=0.9(V_{DD}$ or $V_{DDIO})$, $V_{DDIO}=3V$	-2.5	-5	—	
R_{PH}	Pull-high Resistance for PD2~PD5 Pins (Note)	3V	$V_{DDIO}=V_{DD}$, LVPU=0, PDPU5~2=1	20	60	100	kΩ
		5V	$V_{DDIO}=V_{DD}$, LVPU=0, PDPU5~2=1	10	30	50	
		3V	$V_{DDIO}=V_{DD}$, LVPU=1, PDPU5~2=1	6.67	15	23	
		5V	$V_{DDIO}=V_{DD}$, LVPU=1, PDPU5~2=1	3.5	7.5	12	
I_{LEAK}	Input Leakage Current for PD2~PD5 Pins	5V	$V_{IN}=V_{DD}$ or $V_{IN}=V_{DDIO}$ or $V_{IN}=V_{SS}$	—	—	±1	μA

Note: The R_{PH} internal pull high resistance value is calculated by connecting to ground and enabling the input pin with a pull-high resistor and then measuring pin current at the specified supply voltage level. Dividing the voltage by this measured current provides the R_{PH} value.

Power-on Reset Characteristics

Ta=-40˚C~85˚C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	—	100	mV
RR_{POR}	V_{DD} Rising Rate to Ensure Power-on Reset	—	—	0.035	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	—	—	1	—	—	ms



System Architecture

A key factor in the high-performance features of the Holtek range of microcontrollers is attributed to their internal system architecture. The range of the device take advantage of the usual features found within RISC microcontrollers providing increased speed of operation and enhanced performance. The pipelining scheme is implemented in such a way that instruction fetching and instruction execution are overlapped, hence instructions are effectively executed in one or two cycles for most of the standard or extended instructions respectively, with the exception of branch or call instructions which need one more cycle. An 8-bit wide ALU is used in practically all instruction set operations, which carries out arithmetic operations, logic operations, rotation, increment, decrement, branch decisions, etc. The internal data path is simplified by moving data through the Accumulator and the ALU. Certain internal registers are implemented in the Data Memory and can be directly or indirectly addressed. The simple addressing methods of these registers along with additional architectural features ensure that a minimum of external components is required to provide a functional I/O and A/D control system with maximum reliability and flexibility. This makes the device suitable for low-cost, high-volume production for controller applications.

Clocking and Pipelining

The main system clock, derived from either the HIRC or LIRC oscillator is subdivided into four internally generated non-overlapping clocks, T1~T4. The Program Counter is incremented at the beginning of the T1 clock during which time a new instruction is fetched. The remaining T2~T4 clocks carry out the decoding and execution functions. In this way, one T1~T4 clock cycle forms one instruction cycle. Although the fetching and execution of instructions takes place in consecutive instruction cycles, the pipelining structure of the microcontroller ensures that instructions are effectively executed in one instruction cycle. The exception to this are instructions where the contents of the Program Counter are changed, such as subroutine calls or jumps, in which case the instruction will take one more instruction cycle to execute.

For instructions involving branches, such as jump or call instructions, two machine cycles are required to complete instruction execution. An extra cycle is required as the program takes one cycle to first obtain the actual jump or call address and then another cycle to actually execute the branch. The requirement for this extra cycle should be taken into account by programmers in timing

```
:
:
org 1700h             ; sets initial address of program memory
dc 00Ah,00Bh,00Ch,00Dh,00Eh,00Fh,01Ah,01Bh
:
:
```

In Circuit Programming – ICP

The provision of Flash type Program Memory provides the user with a means of convenient and easy upgrades and modifications to their programs on the same device.

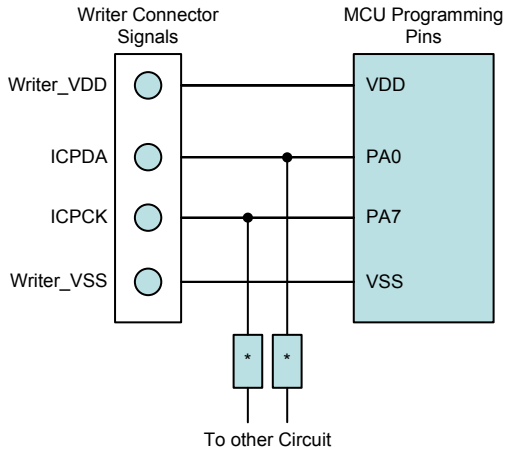
As an additional convenience, Holtek has provided a means of programming the microcontroller in-circuit using a 4-pin interface. This provides manufacturers with the possibility of manufacturing their circuit boards complete with a programmed or un-programmed microcontroller, and then programming or upgrading the program at a later stage. This enables product manufacturers to easily keep their manufactured products supplied with the latest program releases without removal and re-insertion of the device.

The Holtek Flash MCU to Writer Programming Pin correspondence table is as follows:

Holtek Writer Pins	MCU Programming Pins	Pin Description
ICPDA	PA0	Programming Serial Data/Address
ICPCK	PA7	Programming Clock
VDD	VDD	Power Supply (5V)
VSS	VSS	Ground

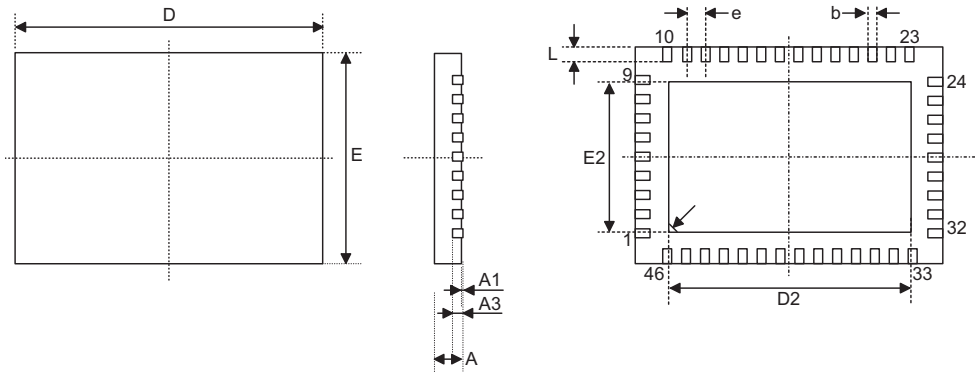
The Program Memory can be programmed serially in-circuit using this 4-wire interface. Data is downloaded and uploaded serially on a single pin with an additional line for the clock. Two additional lines are required for the power supply and one line for the reset. The technical details regarding the in-circuit programming of the device is beyond the scope of this document and will be supplied in supplementary literature.

During the programming process, the user must take care of the ICPDA and ICPCK pins for data and clock programming purposes to ensure that no other outputs are connected to these two pins.



Note: * may be resistor or capacitor. The resistance of * must be greater than 1kΩ or the capacitance of * must be less than 1nF.

SAW Type 46-pin (6.5mm×4.5mm) QFN Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.031	0.033	0.035
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	0.254	0.256	0.258
E	0.175	0.177	0.179
e	—	0.016 BSC	—
D2	0.197	0.201	0.205
E2	0.118	0.122	0.126
L	0.012	0.016	0.020

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	0.00	0.02	0.04
A3	—	0.20 BSC	—
b	0.15	0.20	0.25
D	6.45	6.50	6.55
E	4.45	4.50	4.55
e	—	0.40 BSC	—
D2	5.00	5.10	5.20
E2	3.00	3.10	3.20
L	0.30	0.40	0.50