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JXY

Quick Charge 2.0 ASSP MCU

SFP169

Revision: V0.00 Date: June 26, 2015

Features

CPU Features

- Internal Shunt Regulator output: 3.5V
- Operating Voltage:
  f_{SYS} = 8MHz: 2.2V~5.5V
- Up to 0.5μs instruction cycle with 8MHz system clock at V_{DD}=5V
- Power down and wake-up functions to reduce power consumption
- Two Internal Oscillators – require no external components
  8MHz High Speed Oscillator – HIRC
  32 kHz Low Speed Oscillator – LIRC
- Multi-mode operation: NORMAL, SLOW, IDLE and SLEEP
- All instructions executed in one or two instruction cycles
- Table read instructions
- 63 powerful instructions
- 4-level subroutine nesting
- Bit manipulation instruction

Peripheral Features

- Flash Program Memory: 1K×14
- RAM Data Memory: 64×8
- EEPROM Memory: 32×8
- Watchdog Timer function
- Up to 6 bidirectional I/O lines
- One pin-shared external interrupt
- One 10-bit STM for time measure, compare match output, capture input, PWM output and single pulse output functions
- Dual Time-Base functions for generation of fixed time interrupt signals
- Multi-channel 12-bit resolution A/D converter
- Over Current Protection (OCP) with interrupt
- USB auto detection function
- Low voltage reset function
- Flash program memory can be re-programmed up to 100,000 times
- Flash program memory data retention > 10 years
- EEPROM data memory can be re-programmed up to 1,000,000 times
- EEPROM data memory data retention > 10 years
- Package types: 8-pin SOP-EP

General Description

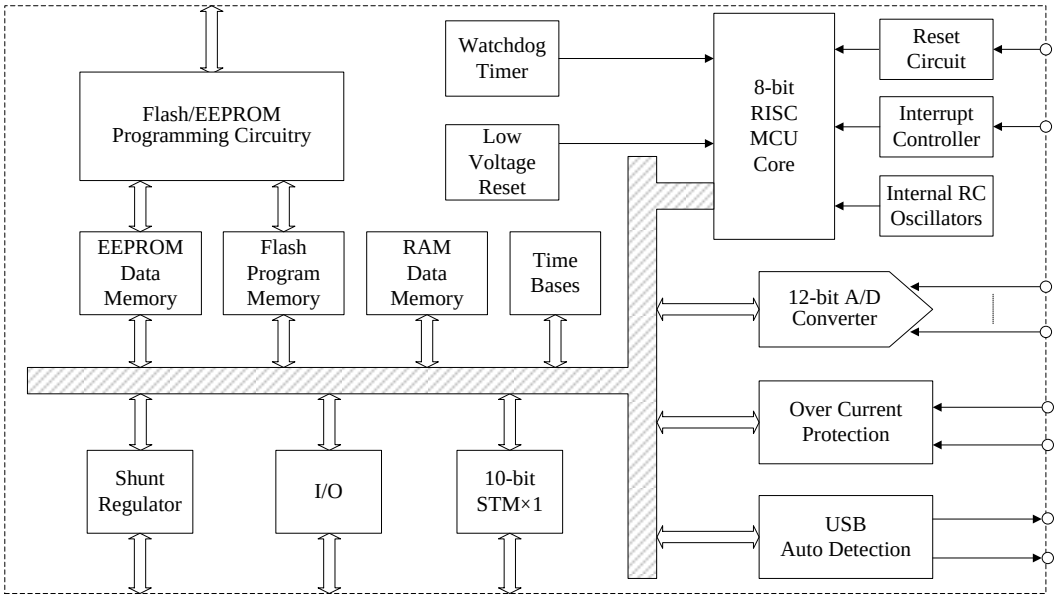
This device is dedicated for use in quick charge 2.0 applications. It is a Flash Memory type 8-bit high performance RISC architecture microcontroller. Offering users the convenience of Flash Memory multi-programming features, the device also includes a wide range of functions and features. Other memory includes an area of RAM Data Memory as well as an area of EEPROM memory for storage of non-volatile data such as serial numbers, calibration data etc.

Analog features include a multi-channel 12-bit A/D converter function, an Over Current Protection function, an USB auto detection function and an internal 3.5V shunt regulator for voltage regulation. One extremely flexible Timer Module provides timing, pulse generation, capture input, compare match output and PWM generation functions. Protective features such as an internal Watchdog Timer and Low Voltage Reset coupled with excellent noise immunity and ESD protection ensure that reliable operation is maintained in hostile electrical environments.

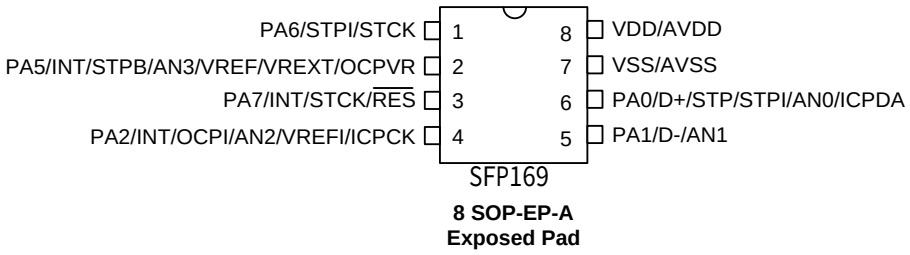
An internal high speed oscillator and an internal low speed oscillator are provided, they are fully integrated system oscillators and require no external components for their implementation.

The inclusion of flexible I/O programming features, Time-Base functions along with many other features ensure that the device will find excellent use in quick charge applications although the device will also lend itself for use in a range of other related applications.

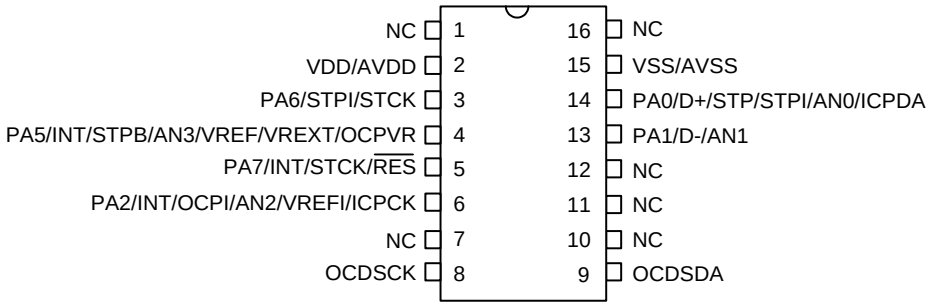
Block Diagram



Pin Assignment



8 SOP-EP-A
Exposed Pad



16 NSOP-A

Note: 1. If the pin-shared pin functions have multiple outputs simultaneously, the desired pin-shared function is determined by the corresponding software control bits.

2. The OCDSDA and OCDSCK pins are supplied for the OCDS dedicated pins and as such are only available for the HT45V0022 EV device.

Pin Description

With the exception of the power pins and some relevant transformer control pins, all pins on the device can be referenced by their Port name, e.g. PA0, PA1 etc, which refer to the digital I/O function of the pins. However these Port pins are also shared with other function such as the Analog to Digital Converter, Timer Module pins etc. The function of each pin is listed in the following table, however the details behind how each pin is configured is contained in other sections of the datasheet.

Note that the pin description refers to the largest package size, as a result some pins may not exist on smaller package types.

Pin Name	Function	OP	I/T	O/T	Description
PA0/D+/STP/[STPI]/ AN0/ICPDA	PA0	PAWU PAPU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	D+	PAS0	—	AN	USB DAC0 output
	STP	PAS0	ST	CMOS	STM output
	STPI	IFS0 PAS0	ST	—	STM input
	AN0	PAS0	AN	—	A/D Converter input channel 0
	ICPDA	—	ST	CMOS	In-circuit programming data/address pin
PA1/D-/AN1	PA1	PAWU	ST	CMOS	General purpose I/O. Register enabled

Pin Name	Function	OP	I/T	O/T	Description
		PAPU PAS0			pull-up and wake-up
	D-	PAS0	—	AN	USB DAC1 output
	AN1	PAS0	AN	—	A/D Converter input channel 1
PA2/[INT]/OCPI/AN2/ VREFI/ICPCK	PA2	PAWU PAPU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	INT	IFS0 PAS0 INTEG	ST	—	External interrupt input
	OCPI	PAS0	AN	—	Over current protection input
	AN2	PAS0	AN	—	A/D Converter input channel 2
	VREFI	PAS0	AN	—	PGA input for A/D Converter reference
	ICPCK	—	ST	CMOS	In-circuit programming clock pin
PA5/INT/STPB/AN3/ VREF/VREXT/OCPVR	PA5	PAWU PAPU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	INT	IFS0 PAS1 INTEG	ST	—	External interrupt input
	STPB	PAS1	ST	CMOS	STM inverting output
	AN3	PAS1	AN	—	A/D Converter input channel 3
	VREF	PAS1	AN	—	A/D Converter reference input
	VREXT	PAS1	AN	—	USB DAC0/1 reference input
	OCPVR	PAS1	AN	—	Over current protection reference input
PA6/STPI/[STCK]	PA6	PAWU PAPU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	STPI	IFS0 PAS1	ST	—	STM input
	STCK	IFS0 PAS1	ST	—	STM clock input
PA7/[INT]/STCK/ $\overline{\text{RES}}$	PA7	PAWU PAPU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	INT	IFS0 PAS1 INTEG	ST	—	External interrupt input
	STCK	IFS0 PAS1	ST	—	STM clock input
	$\overline{\text{RES}}$	PAS1 RSTC	ST	—	External reset input
VDD/AVDD	VDD	—	PWR	—	Digital positive power supply
	AVDD	—	PWR	—	Analog positive power supply
VSS/AVSS	VSS	—	PWR	—	Digital negative power supply
	AVSS	—	PWR	—	Analog negative power supply
The following pins are only for the HT45V0022					
NC	NC	—	—	—	No connection
OCDSCK	OCDSCK	—	ST	—	OCDS Clock Line for EV device only
OCDSDA	OCDSDA	—	ST	CMOS	OCDS Data/Adress Line for EV device only

Legend: I/T: Input type; O/T: Output type
OP: Optional register option
PWR: Power; ST: Schmitt Trigger input
CMOS: CMOS output; AN: Analog Signal

Absolute Maximum Ratings

Supply Voltage..... V_{SS}-0.3V to V_{SS}+6.0V
Input Voltage..... V_{SS}-0.3V to V_{DD}+0.3V
Storage Temperature..... -50℃ to 125℃
Operating Temperature..... -40℃ to 85℃
I_{OL} Total..... 80mA
I_{OH} Total..... -80mA
Total Power Dissipation..... 500mW

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta = 25℃

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage (HIRC)	—	f_{SYS}=8MHz	2.2	—	5.5	V
I_{DD}	Operating Current (HIRC)	3V	No load, f_{SYS} = f_{HIRC}= 8MHz, All peripherals off, WDT enable, LVR enable	—	1.0	2.0	mA
		5V		—	2.0	3.0	mA
		3V	No load, f_{SYS} = f_{HIRC}/2, All peripherals off, WDT enable, LVR enable	—	1.0	1.5	mA
		5V		—	1.5	2.0	mA
		3V	No load, f_{SYS} = f_{HIRC}/4, All peripherals off, WDT enable, LVR enable	—	0.9	1.3	mA
		5V		—	1.3	1.8	mA
		3V	No load, f_{SYS} = f_{HIRC}/8, All peripherals off, WDT enable, LVR enable	—	0.8	1.1	mA
		5V		—	1.1	1.6	mA
		3V	No load, f_{SYS} = f_{HIRC}/16, All peripherals off, WDT enable, LVR enable	—	0.7	1.0	mA
		5V		—	1.0	1.4	mA
		3V	No load, f_{SYS} = f_{HIRC}/32, All peripherals off, WDT enable, LVR enable	—	0.6	0.9	mA
		5V		—	0.9	1.2	mA
		3V	No load, f_{SYS} = f_{HIRC}/64, All peripherals off, WDT enable, LVR enable	—	0.5	0.8	mA
		5V		—	0.8	1.1	mA
	Operating Current (LIRC)	3V	No load, f_{SYS} = f_{LIRC} = 32kHz, All peripherals off, WDT enable, LVR enable	—	20	30	μA
		5V		—	30	60	μA
I_{STB}	Standby Current (SLEEP mode)	3V	No load, All peripherals off, WDT disable	—	0.2	0.8	μA
		5V		—	0.5	1	μA
	Standby Current (SLEEP mode)	3V	No load, All peripherals off, WDT enable	—	1.5	3	μA
		5V		—	3	5	μA
	Standby Current (IDLE0 mode)	3V	No load, All peripherals off, f_{SUB} on	—	3	5	μA
		5V		—	5	10	μA
	Standby Current (IDLE1 mode)	3V	No load, f_{SYS} = f_{HIRC}/2 = 4MHz, All peripherals off, f_{SUB} on	—	180	250	μA
		5V		—	400	600	μA
		3V	No load, f_{SYS} = f_{HIRC} = 8MHz, All peripherals off, f_{SUB} on	—	360	500	μA
		5V		—	600	800	μA
V_{IL}	Input Low Voltage for I/O Ports or Input	5V	—	0	—	1.5	V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
	Pins except $\overline{RES}$ pin	—	—	0	—	$0.2V_{DD}$	V
	Input Low Voltage for $\overline{RES}$ pin	—	—	0	—	$0.4V_{DD}$	V
V_{IH}	Input High Voltage for I/O Ports or Input	5V	—	3.5	—	5.0	V
	Pins except $\overline{RES}$ pin	—	—	$0.8V_{DD}$	—	V_{DD}	V
	Input High Voltage for $\overline{RES}$ pin	—	—	$0.9V_{DD}$	—	V_{DD}	V
I_{OL}	I/O Port Sink Current	3V	$V_{OL}=0.1V_{DD}$	18	36	—	mA
		5V		40	80	—	mA
I_{OH}	I/O Port Source Current	3V	$V_{OH}=0.9V_{DD}$	-3	-6	—	mA
		5V		-7	-14	—	mA
I_{OCDS}	Operating Current (Normal Mode)	3V	No load, $f_{SYS}=f_{HIRC}$=8MHz, All peripherals off, WDT enable	—	1.4	2.0	mA
I_{LEAK}	Input Leakage Current	3V	$V_{IN}=V_{DD}$ or $V_{IN}=V_{SS}$	—	—	±1	μA
		5V		—	—	±1	μA
R_{PH}	Pull-high Resistance for I/O Ports (OCDSCK and OCDSDA for HT45V0022)	3V	—	20	60	100	kΩ
		5V	—	10	30	50	kΩ

A.C. Characteristics

Ta = 25℃

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
f_{CPU}	Operating Clock	2.2V~5.5V	—	DC	—	8	MHz
f_{HIRC}	High Speed Internal RC Oscillator (HIRC)	3V/5V	Ta = 25℃	-2%	8	+2%	MHz
		3V/5V	Ta = 0℃ ~70℃	-5%	8	+5%	MHz
		2.2V~5.5V	Ta = 0 ℃ ~70℃	-8%	8	+8%	MHz
		2.2V~5.5V	Ta = -40℃ ~ 85℃	-12%	8	+12%	MHz
f_{LIRC}	Low Speed Internal RC Oscillator (LIRC)	2.2V~5.5V	Ta = -40℃ ~ 85℃	8	32	50	kHz
t_{TIMER}	STCK and STPI Input Pin Minimum Pulse Width	—	—	0.3	—	—	μs
t_{RES}	External Reset Minimum Low Pulse Width	—	—	10	—	—	μs
t_{INT}	External Interrupt Minimum Pulse Width	—	—	10	—	—	μs
t_{RSTD}	System Reset Delay Time (Power-on reset, LVR hardware reset, WDT software reset (WDTC), RSTC software reset)	—	—	25	50	100	ms
	System Reset Delay Time ($\overline{RES}$ pin reset, WDT time-out hardware cold reset)	—	—	8.3	16.7	33.3	ms
t_{SST}	System Start-up Timer Period (wake-up from power-down and f_{SYS} off at power-down)	—	$f_{SYS}=f_{HIRC}$ ~f_{HIRC}/64	16	—	—	t_{HIRC}
		—	$f_{SYS}=f_{LIRC}$	2	—	—	t_{LIRC}
	System Start-up Timer Period (slow mode ↔ normal mode)	—	f_{HIRC} off → on (HIRCF = 1)	16	—	—	t_{HIRC}
	System Start-up Timer Period (wake-up from power-down and f_{SYS} on at power-down)	—	$f_{SYS}=f_{HIRC}$ ~ f_{HIRC}/64	2	—	—	t_{HIRC}
		—	$f_{SYS}=f_{LIRC}$	2	—	—	t_{LIRC}
	System Start-up Timer Period (WDT time-out hardware cold reset)	—	—	0	—	—	t_H

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
t_{EERD}	EEPROM Read Time	—	—	—	—	4	t_{SYS}
t_{EEWR}	EEPROM Write Time	—	—	—	2	4	ms

A/D Converter Electrical Characteristics

Operating Temperature: -40℃~85℃, unless otherwise specify

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	A/D Converter Operating Voltage	—	—	2.7	—	5.5	V
V_{ADI}	A/D Converter Input Voltage	—	—	0	—	V_{REF}	V
V_{REF}	A/D Converter Reference Voltage	—	—	2	—	V_{DD}	V
DNL	Differential Non-linearity	3V	SAINS[3:0] = 0000B, SAVRS[1:0] = 01B, V_{REF}=V_{DD}, t_{ADCK} =0.5μs	—	—	±3	LSB
		5V					
		3V	SAINS[3:0] = 0000B, SAVRS[1:0] = 01B, V_{REF}=V_{DD}, t_{ADCK} =10μs	—	—	±3	LSB
		5V					
INL	Integral Non-linearity	3V	SAINS[3:0] = 0000B, SAVRS[1:0] = 01B, V_{REF}=V_{DD}, t_{ADCK} =0.5μs	—	—	±4	LSB
		5V					
		3V	SAINS[3:0] = 0000B, SAVRS[1:0] = 01B, V_{REF}=V_{DD}, t_{ADCK} =10μs	—	—	±4	LSB
		5V					
I_{ADC}	Additional Current for A/D Converter Enable	3V	No load, t_{ADCK} =0.5μs	—	0.2	0.4	mA
		5V	No load, t_{ADCK} =0.5μs	—	0.3	0.6	mA
t_{ADCK}	A/D Converter Clock Period	—	—	0.5	—	10	μs
t_{ADC}	A/D Conversion Time (Include Sample and Hold Time)	—	—	—	16	—	t_{ADCK}
t_{ON2ST}	A/D Converter On-to-Start Time	—	—	4	—	—	μs
I_{PGA}	Additional Current for PGA Enable	3V	No load	–	270	550	μA
		5V	No load	–	270	550	μA
V_{CM}	PGA Common Mode Voltage Range	3V	—	V_{SS}	—	V_{DD}	V
		5V	—	V_{SS}	—	V_{DD}	V
V_{OR}	PGA Maximum Output Voltage Range	3V	—	V_{SS} + 0.1	—	V_{DD} - 0.1	V
		5V	—	V_{SS} + 0.1	—	V_{DD} - 0.1	V
Ga	PGA Gain Accuracy	—	Gain=1, 2, 3, 4 V_{RI} > 0.2V	-5	—	+5	%

LVR Electrical Characteristics

Ta = 25℃

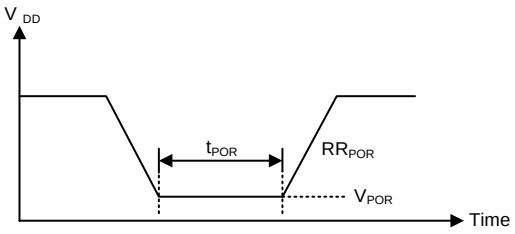
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	1.9	—	5.5	V
V_{LVR}	Low Voltage Reset Voltage	—	LVR Enable	-5%	2.1	+5%	V
t_{LVR}	Low Voltage Width to Reset	—	—	160	320	640	μs

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
		5V	—	—	5	—	KΩ
OSRR	Offset Error	3V	$V_{REF} = V_{DD} = 3V$ Data word = 128	—	—	50	mV
		5V	$V_{REF} = V_{DD} = 5V$ Data word = 128	—	—	80	mV
GERR	Gain Error	3V	$V_{REF} = V_{DD} = 3V$ Data word = 128	—	—	50	mV
		5V	$V_{REF} = V_{DD} = 5V$ Data word = 128	—	—	80	mV
R_{ON}	Analog Switch On Resistance between D+ and D-	5V	—	—	125	200	Ω
R_{PL}	Pull-low Resistance for D+, D-	5V	—	400	700	1400	kΩ
ERR	The Rrror for D+, D- Output Voltage	5V	DAC reference = V_{DD}, DAC digital value = 148, D+, D- connect 150kΩ to ground	2.57	2.7	2.84	V
		5V	DAC reference = V_{DD}, DAC digital value = 110, D+, D- connect 150kΩ to ground	1.9	2.0	2.1	V
R_D	The Sum of Dx_R1and Dx_R2	3V	—	2	4	6	kΩ
		5V	—	2	4	6	kΩ
RR_D	The Ratio of Dx_R1/Dx_R2	3V	—	-2%	1:1	+2%	—
		5V	—	-2%	1:1	+2%	—
R_{PH}	Pull-high Resistance for I/O Ports	3V	—	20	60	100	kΩ
		5V	—	10	30	50	kΩ

Power on Reset Electrical Characteristics

Ta = 25℃

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	—	100	mV
RR_{POR}	V_{DD} Rising Rate to Ensure Power-on Reset	—	—	0.035	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	—	—	1	—	—	ms



System Architecture

A key factor in the high-performance features of the Holtek range of microcontrollers is attributed to their internal system architecture. The device takes advantage of the usual features found within RISC microcontrollers providing increased speed of operation and Periodic performance. The pipelining scheme is implemented in such a way that instruction fetching and instruction execution are overlapped, hence instructions are effectively executed in one cycle, with the exception of branch or call instructions. An 8-bit wide ALU is used in practically all instruction set operations, which carries out arithmetic operations, logic operations, rotation, increment, decrement, branch decisions, etc. The internal data path is simplified by moving data through the Accumulator and the ALU. Certain internal registers are implemented in the Data Memory and can be directly or indirectly addressed. The simple addressing methods of these registers along with additional architectural features ensure that a minimum of external components is required to provide a functional I/O and A/D control system with maximum reliability and flexibility. This makes the device suitable for low-cost, high-volume production for controller applications

Clocking and Pipelining

The main system clock, derived from either a HIRC or LIRC oscillator is subdivided into four internally generated non-overlapping clocks, T1~T4. The Program Counter is incremented at the beginning of the T1 clock during which time a new instruction is fetched. The remaining T2~T4 clocks carry out the decoding and execution functions. In this way, one T1~T4 clock cycle forms one instruction cycle. Although the fetching and execution of instructions takes place in consecutive instruction cycles, the pipelining structure of the microcontroller ensures that instructions are effectively executed in one instruction cycle. The exception to this are instructions where the contents of the Program Counter are changed, such as subroutine calls or jumps, in which case the instruction will take one more instruction cycle to execute.

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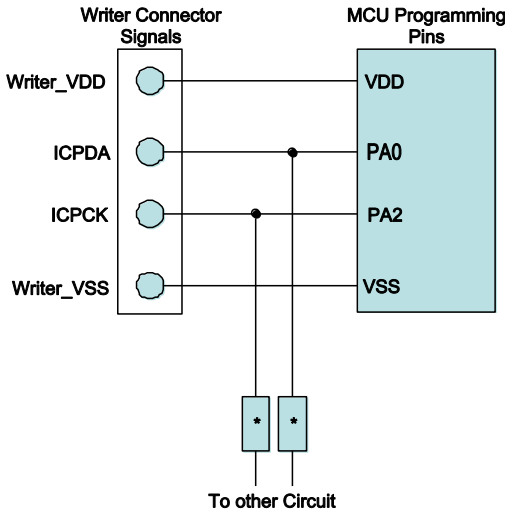
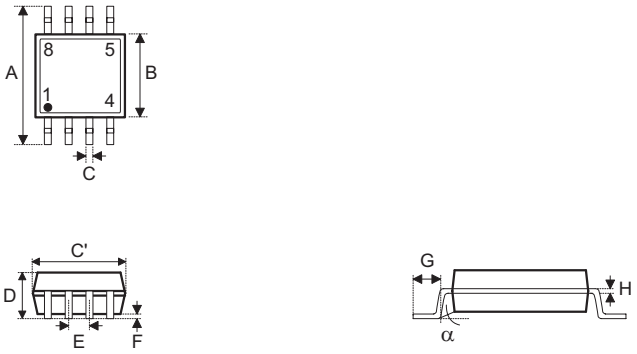


Note: * may be resistor or capacitor. The resistance of * must be greater than 1kΩ or the capacitance of * must be less than 1nF.

為方便調試，以及後續程序升級，請務必預留相應的燒錄點在PCBA上。

Holtek e-Link Pins	EV Chip Pins	Pin Description
OCDSDA	OCDSDA	On-chip Debug Support Data/Address input/output
OCDSCK	OCDSCK	On-chip Debug Support Clock input
VDD	VDD	Power Supply
GND	VSS	Ground

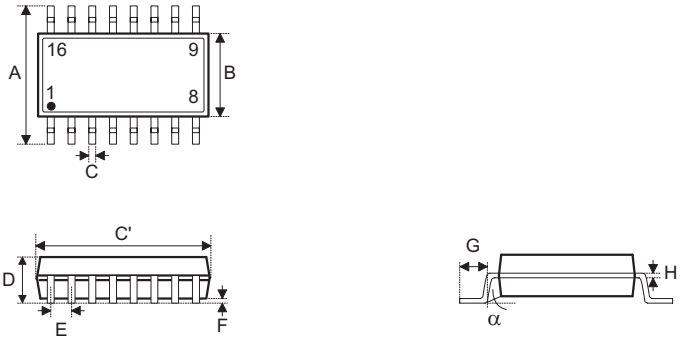
8-pin SOP (150mil) 外形尺寸



符号	尺寸（单位：inch)		
	最小	正常	最大
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C′	—	0.193 BSC	—
D	—	—	0.069
E	—	0.050 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

符号	尺寸（单位：mm)		
	最小	正常	最大
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.31	—	0.51
C′	—	4.90 BSC	—
D	—	—	1.75
E	—	1.27 BSC	—
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

16-pin NSOP (150mil) 外形尺寸



符号	尺寸（单位：inch)		
	最小	正常	最大
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C’	—	0.390 BSC	—
D	—	—	0.069
E	—	0.050 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

符号	尺寸（单位：mm)		
	最小	正常	最大
A	—	6.0 BSC	—
B	—	3.9 BSC	—
C	0.31	—	0.51
C’	—	9.9 BSC	—
D	—	—	1.75
E	—	1.27 BSC	—
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°